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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,094	09/28/2001	Siddhartha Bhowmik	Bhowmik 12-146-1/075903-3	7197

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EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/967,094	Applicant(s) BHOWMIK ET AL.
	Examiner Fazli Erdem	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12 and 17-19* is/are rejected.

7)☒ Claim(s) *6 and 13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Allowable Subject Matter

1. Claims 6 and 13-16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,7, 8, and 17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (US 2002/0132473 A1) in view of Maydan et al. (6,372,633) further in view of Lin et al. (5,985,749) further in view of Trivedi et al (5,981,380) further in view of Chang (6,037,263).

Regarding Claims 1, 7, 8, and 17-19. Chiang et al. disclose integrated barrier layer structure for copper contact level metallization where a method for forming an integrated barrier layer structure that is compatible with copper (Cu) metallization schemes for integrated circuit fabrication is shown. An integrated circuit is metallized by forming an integrated barrier layer structure on a silicon substrate followed by a deposition of one or more copper layers. The integrated barrier layer structure includes one or more barrier layers selected from tantalum, tantalum nitride, tungsten and tungsten nitride, conformably deposited on the silicon substrate.

After the one or more barrier layers are deposited on the silicon substrate, the silicon substrate is heated to form a silicide layer at the interface between the silicon substrate and the barrier layers Chiang et al. fail to disclose the required tungsten barrier layer and tungsten plug and the required method of making such structure. However, Maydan et al. disclose a method an apparatus for forming metal interconnects where the required tungsten barrier layer and the required tungsten plug structures are shown. Furthermore, Lin et al. discloses a method of forming a via hole structure including CVD tungsten silicide barrier layer where in Fig. 2(A) a metal layer is formed on a sidewall and a bottom surface of the via hole, a tungsten silicide barrier layer is formed on the first metal layer by chemical vapor deposition and the via hole is subsequently filled with a metal. Lin et al. use tungsten silicide and titanium compound as the first and the second barrier layers. Lin et al. also do not specifically show the substrate. However, Trivedi et al. disclose a method of forming a local interconnect including selectively etched conductive layers and recess formation where usage of tungsten and tungsten silicide as the first and the second barrier layers respectively explained. Furthermore Chang discloses a plasma enhanced CVD deposition of tungsten and tungsten compounds where the substrate is specifically showed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required tungsten barrier layer and tungsten plug structures and required manufacturing method as taught by Maydan et al. and Lin et al., Trivedi et al., Chang combination in Chiang et al. in order to have a semiconductor device with more reliability

3. Claims 2, 3, 4, 5, 9, 10, 11 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. (US 2002/0132473 A1) in view of Maydan et al. (6,372,633) further in view of Lin et al. (5,985,749) further in view of Trivedi et al (5,981,380) further in view of Chang (6,037,263) further in view of Cadien et al. (5,604,158) further in view of Asahina et al. (6,144,097).

Regarding Claims 2, 3, 4, 5, 9, 10, 11 and 12, Chiang et al. disclose integrated barrier layer structure for copper contact level metallization where a method for forming an integrated barrier layer structure that is compatible with copper (Cu) metallization schemes for integrated circuit fabrication is shown. An integrated circuit is metallized by forming an integrated barrier layer structure on a silicon substrate followed by a deposition of one or more copper layers. The integrated barrier layer structure includes one or more barrier layers selected from tantalum, tantalum nitride, tungsten and tungsten nitride, conformably deposited on the silicon substrate. After the one or more barrier layers are deposited on the silicon substrate, the silicon substrate is heated to form a silicide layer at the interface between the silicon substrate and the barrier layers Chiang et al. fail to disclose the required tungsten barrier layer and tungsten plug and the required method of making such structure. However, Maydan et al. disclose a method an apparatus for forming metal interconnects where the required tungsten barrier layer and the required tungsten plug structures are shown.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required tungsten plug and tungsten barrier layers structures in Chiang et al. as taught by Maydan et al. in order to have a barrier layer and plug structures having better performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE
March 24, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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